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Comments:

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Application Serial No.: 10/674,085 Filed: September 29, 2003

Patent No: 7,093,220 Issued: August 15, 2006

Inventors: Elias L. FALLON et al.

Art Unit: 2825

Examiner: Y. Rossoshek

Title: METHOD FOR GENERATING CONSTRAINED COMPONENT PLACEMENT FOR INTERGRATED CIRCUITS AND PACKAGES

Enclosed are the following documents:

1. Transmittal - 1 page

2. Request for Withdrawal as Attorney or Agent and Change of

Correspondence Address - 1 page

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FORM		First Named Inventor	Elias L. FALLON				
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(to be used for ell correspondence after	rinitial filing)	Examiner Name	Y. Rossoshek				
Total Number of Pages in This Submiss		Attorney Docket Numb	er 188122003600				
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